

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 789 450 A2

EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.08.1997 Bulletin 1997/33

(51) Int Cl.⁶ H03F 1/02

(21) Application number: 97300525.9

(22) Date of filing: 28.01.1997

(84) Designated Contracting States:
FR GB IT NL SE

(72) Inventor: Karanicolas, Andrew N.
Morganville, New Jersey 07751 (US)

(30) Priority 07.02.1996 US 597776

(74) Representative:
Buckley, Christopher Simon Thirsk et al
Lucent Technologies (UK) Ltd,
5 Mornington Road
Woodford Green, Essex IG8 0TU (GB)

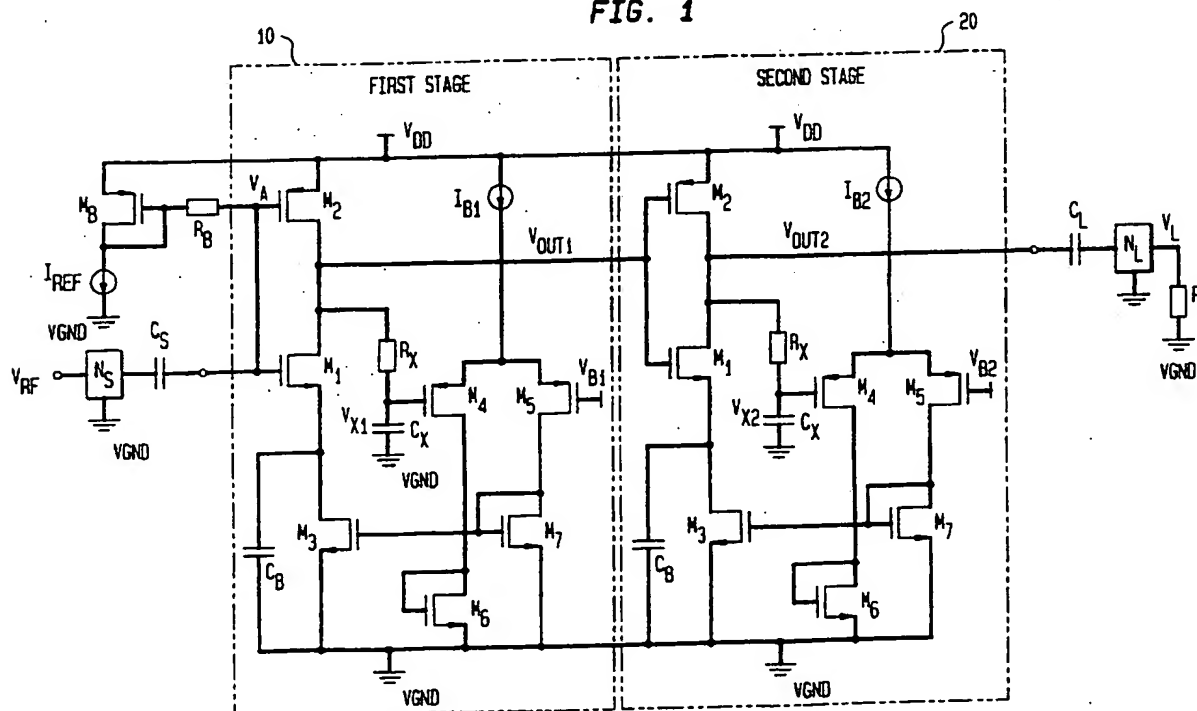
(71) Applicant LUCENT TECHNOLOGIES INC.
Murray Hill, New Jersey 07974-0636 (US)

(54) An efficient RF CMOS amplifier with increased transconductance

(57) An RF IC having an improved transconductance comprises a first active device (M_1) of a first conductance type having a gate, a drain and a source, and a second active device (M_2) of a second conductance type having a gate, a drain and a source. The second active device is coupled in series with the first active device. The gate of the first active device is coupled to the

gate of the second active device. A current reuse circuit (M_3 to M_8) is coupled to the first active device and the second active device wherein a current flowing from the drain of the first active device is reused in the second active device whereby transconductance is increased without an increased current utilization and without an increase in noise.

FIG. 1



a cascade connection of two transconductance amplifier stages. One advantage of the two-stage design is that reverse isolation of the LNA is improved in comparison to a single stage design. Another advantage is that by decoupling the input and output ports matching is simplified. An RF signal is applied at V_{RF} , which drives MOS gates M_1 and M_2 in the first stage. Since an external image rejection filter is typically used between the LNA output and the mixer RF input, the LNA output is capable of driving a load resistance R_L of 50 Ω .

As the first and second stage topologies are identical, only the operation of the first stage (single stage) is described herein. Again referring to FIG. 1, devices M_1 and M_2 are configured such that the transconductance of the stage is $g_m = g_{m1} + g_{m2}$, where g_{m1} is the transconductance of M_1 and g_{m2} is the transconductance of M_2 . Capacitor C_B shunts the source of M_1 to ground at high frequencies. Since the drain current of M_1 is reused in M_2 , g_m increases without increasing current consumption, in contrast to a common source amplifier composed of M_1 or M_2 alone. A bias feedback amplifier sets the dc output voltage V_{OUT1} of the stage to the bias reference V_{B1} . Devices M_3 , M_4 , M_5 , M_6 and M_7 steer bias current into devices M_1 and M_2 . The bias reference I_{REF} and the current mirror which is composed of devices M_8 and M_2 establish the desired bias current in devices M_1 and M_2 . The bias feedback loop is completed with a low pass filter comprised of R_X and C_X . The low pass filter provides dc output voltage V_{X1} from V_{OUT1} . The low frequency pole that is contributed by the filter dominates the bias feedback amplifier loop transmission to achieve a high phase margin for the loop. Direct coupling is utilized between the output of the first stage and the input of the second stage. The bias reference V_{B1} sets the dc output voltage V_{OUT1} for the first stage and thus sets the dc input voltage of the second stage, determining the second stage bias current. The second stage bias feedback amplifier sets the dc output voltage V_{OUT2} to bias reference V_{B2} . Where V_A is the dc input voltage of the first stage determined by I_{REF} $V_{B1} = V_{B2} = V_A$. Resistors R_B and R_X are chosen sufficiently large to prevent significant input and output loading.

Referring to FIG. 2 there is shown a schematic of a mixer according to the present invention. The mixer 30 comprises of 4 nMOS devices M_{13} , M_{14} , M_{19} , and M_{20} , 5 pMOS devices M_{11} , M_{12} , M_{15} , M_{17} , and M_{21} , resistors R_{X1} , R_{X2} , R_{B1} and R_{B2} capacitor C_X , and current sources I_B and I_{REF} . The gate of M_{11} is coupled to the gate of M_{14} and V_{LO1} . The gate of M_{13} is coupled to the gate of M_2 and V_{LO2} . The source of M_{16} , the source of M_{18} , and current source I_B are coupled to a supply voltage V_{DD} . The gate of M_{16} is coupled to V_{REF1} . The gate of M_{18} is coupled to the drain of M_{18} . Current source I_{REF} is coupled between the drain of M_{18} and supply voltage V_{GND} . Resistor R_{B1} is coupled between the gate of M_{16} and the gate of M_{18} . The drain of M_{16} is coupled between the source of M_{13} and the source of M_{14} . The drain of M_{13} is coupled to the drain of M_{11} . The drain of M_{14} is

coupled to the drain of M_{12} . The source of M_{11} and the source of M_{12} are coupled to the drain of M_{15} . The drain of M_{15} is coupled to V_{GND} . R_{X1} is coupled between the drain of M_{14} and the gate of M_{19} . The voltage at the gate of M_{19} is called V_X . R_{X2} is coupled between the drain of M_{11} and the gate of M_{19} . C_X is coupled between the gate of M_{19} and V_{GND} . The drain of M_{11} is coupled to V_{OUT2} . The drain of M_{14} is coupled to V_{OUT1} . The current source is coupled to the source of M_{19} and the source of M_{20} . The drain of M_{19} is coupled to the drain of M_{21} and the gate of M_{21} . The drain of M_{20} is coupled to the drain of M_{17} and the gate of M_{17} . R_{B2} is coupled between the gate of M_{15} and the gate of M_{17} . The source of M_{17} , the source of M_{21} , and the source of M_{15} are coupled to V_{GND} .

External networks N_S matches the mixer R_F port to 50 Ω . The RF input is applied at V_{RF} , driving V_{RF1} and V_{RF2} , and in turn gates M_{15} and M_{16} , in phase. Again referring to FIG. 2, devices M_{15} and M_{16} are configured as a transconductance amplifier where $g_m = g_{m15} + g_{m16}$, where g_{m15} is the transconductance of M_{15} and g_{m16} is the transconductance of M_{16} . The mixer amplifier uses the design principle used for the LNA stages such that g_m is increased while the drain current is reused, thus avoiding increased current consumption for increased g_m . The cross coupled devices M_{11} , M_{12} , M_{13} and M_{14} comprise the main mixer cell which is driven by the differential local oscillator (LO) inputs V_{LO1} and V_{LO2} . The drain currents of devices M_{15} and M_{16} are steered through devices M_{11} and M_{13} or through devices M_{12} and M_{14} , as a function of the LO phase. When an input V_{RF} is applied, the drain currents of M_{15} and M_{16} differ by $g_m V_{RF}$. This difference current is then chopped by the mixer cell resulting in the desired IF current at the output ports V_{OUT1} and V_{OUT2} of the mixer. The high impedance mixer outputs are capable of driving an external high impedance IF filter.

Biasing of the mixer is similar to that used for the LNA stages. A common mode feedback amplifier sets the dc common mode output level of the mixer, V_X , to the bias reference, V_B . A differential pair and current mirror are comprised of MOS devices M_{15} , M_{17} , M_{19} , M_{20} , and M_{21} , which steer the bias current into the mixer cell. Bias reference I_{REF} and a current mirror comprised of MOS devices M_8 and M_{16} establish the desired bias current in the mixer cell. A low pass filter completes the feedback loop. The low pass filter is comprised of R_{X1} , R_{X2} and C_X . This provides the dc common mode level V_X from outputs V_{OUT1} and V_{OUT2} . Resistors R_{B1} , R_{B2} , R_{X1} and R_{X2} are selected sufficiently large to prevent significant input and output loading.

Referring to FIG. 3 there is shown a graph of the measured LNA forward and reverse gain magnitudes, $|S_{21}|$ and $|S_{12}|$, respectively.

Referring to FIG. 4 there is shown a graph of the measured mixer IF output spectrum when a two tone RF input at 899.5 Mhz and 900.5 Mhz is mixed with a LO frequency at 1 Ghz. The RF power level is 29 dBm for

FIG. 1

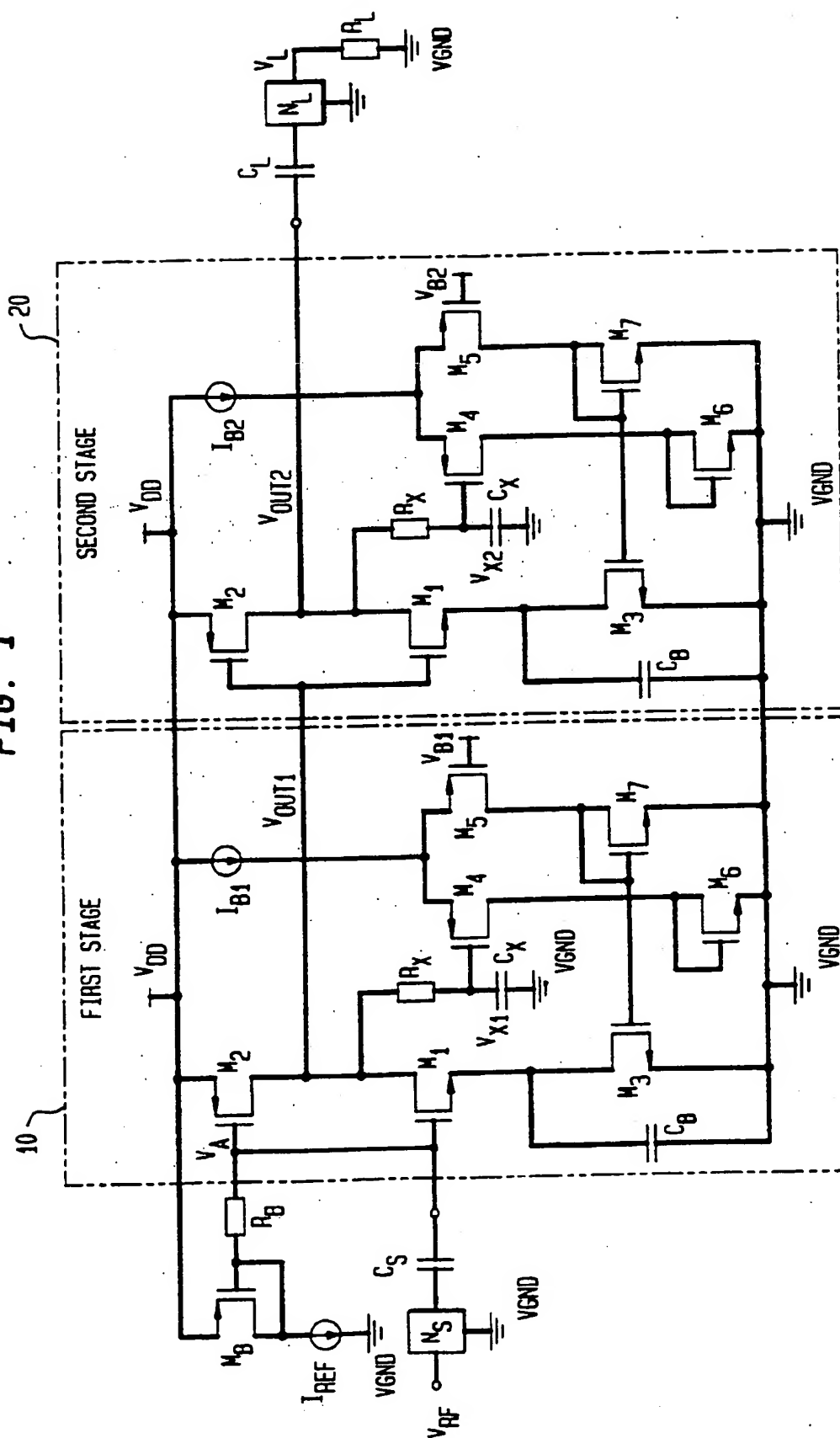


FIG. 3

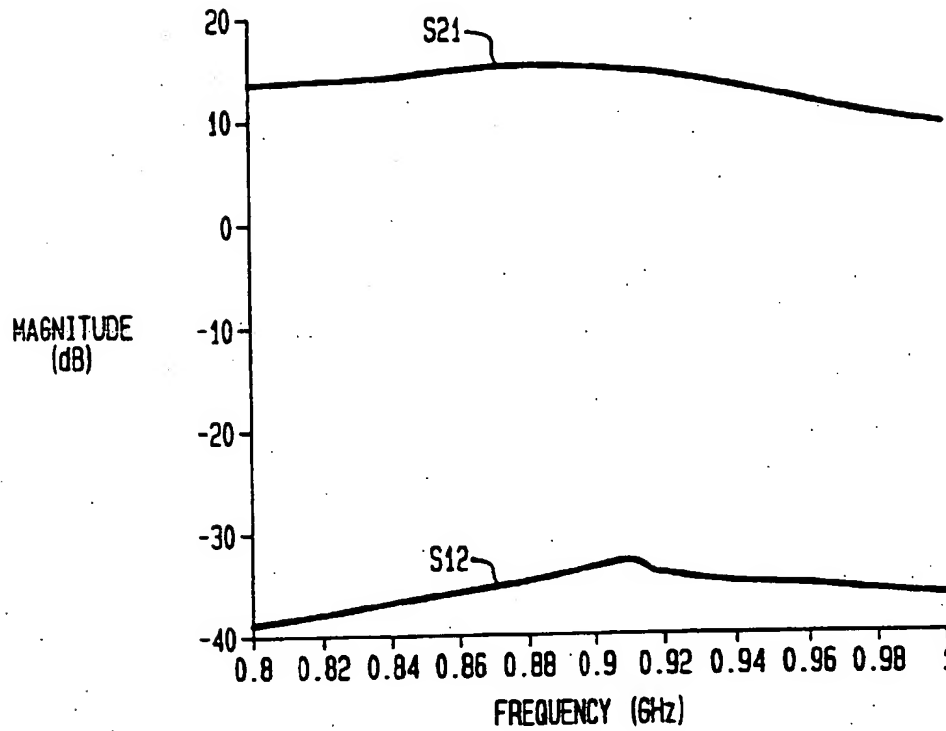
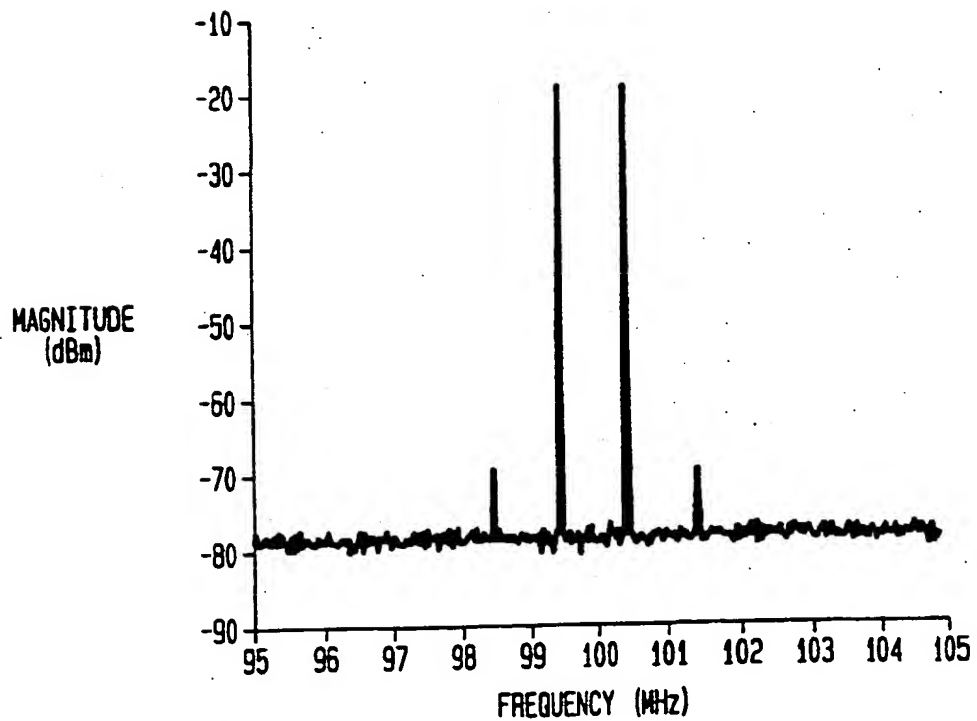


FIG. 4



EUROPEAN PATENT APPLICATION

(51) Int Cl.⁶: **H03F 1/02**

(22) Date of filing: 28.01.1997

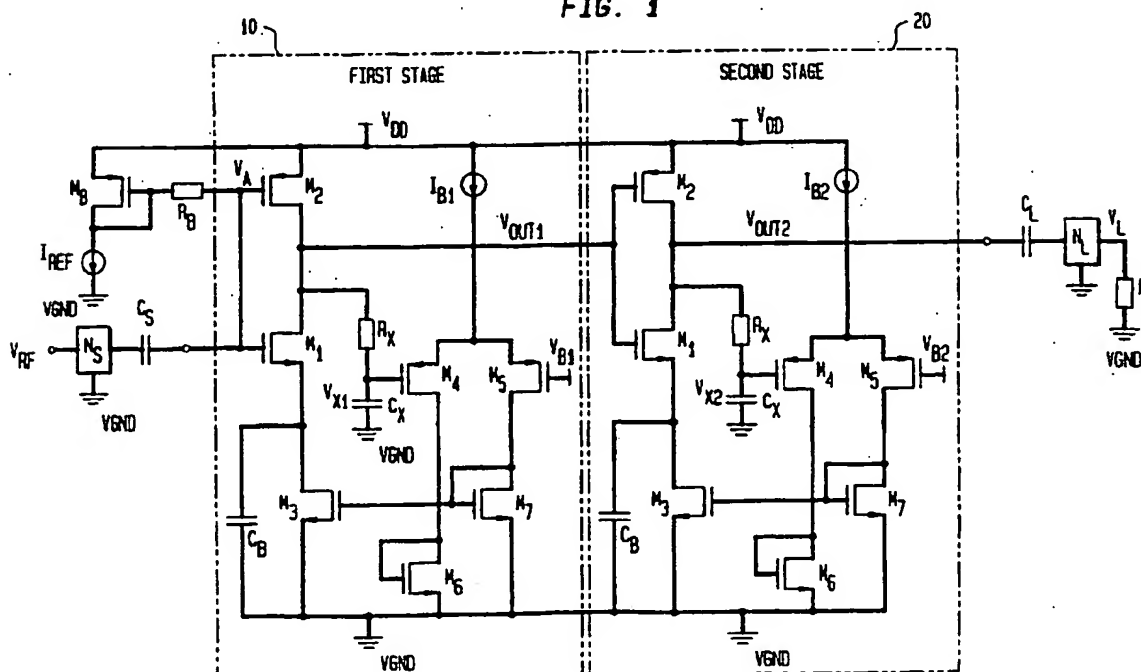
(72) Inventor: Karanicolas, Andrew N.
Morganville, New Jersey 07751 (US)

(74) Representative:
Buckley, Christopher Simon Thlrsk et al
Lucent Technologies (UK) Ltd,
5 Mornington Road
Woodford Green, Essex IG8 0TU (GB)

(54) **An efficient RF CMOS amplifier with increased transconductance**

gate of the second active device. A current reuse circuit (M_3 to M_8) is coupled to the first active device and the second active device wherein a current flowing from the drain of the first active device is reused in the second active device whereby transconductance is increased without an increased current utilization and without an increase in noise.

FIG. 1



**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 97 30 0525

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

20-05-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0480815 A	15-04-1992	FR 2667743 A	10-04-1992
		DE 69105905 D	26-01-1995
		DE 69105905 T	04-05-1995
		US 5221910 A	22-06-1993
EP 0318263 A	31-05-1989	US 4797631 A	10-01-1989
		DE 3852930 D	16-03-1995
		DE 3852930 T	24-05-1995
		JP 1188111 A	27-07-1989
		JP 2597690 B	09-04-1997
		KR 9705287 B	15-04-1997
DE 4126061 A	26-03-1992	DD 295443 A	31-10-1991